AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISION TO 37 CFR 1.121)

Please add new claims 21-26.

1. (CURRENTLY AMENDED) An apparatus comprising:

a first device comprising (i) a first gate configured to receive an input voltage ranging from up to twice a first supply voltage with respect to a second supply voltage to at least said second supply voltage, (ii) a first drain configured to receive said first supply voltage, and (iii) a first source coupled to a first output; and

a first resistive element having (i) a first side coupled to said first source and (ii) a second side configured to receive said second supply voltage, wherein said apparatus is arranged such that a maximum voltage drop across a gate oxide of said first device does not exceed a difference between said first supply voltage and said second supply voltage and a voltage drop from said first gate to said first output is non-linear as a function of said input voltage.

2. (PREVIOUSLY CANCELLED)

3. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said first device is configured in a source-follow configuration.

4. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said first device comprises an NMOS device.

5. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said first device comprises a native NMOS device.

6. (PREVIOUSLY CANCELLED)

7. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said first device comprises a PMOS device.

8. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said first device comprises a native PMOS device.

9. (ORIGINAL) The apparatus according to claim 1, wherein said first supply voltage comprises a ground voltage.

10. (ORIGINAL) The apparatus according to claim 1, wherein said second supply voltage comprises a ground voltage.

11. (CURRENTLY AMENDED) A method for implementing voltage protection comprising the steps of:

configuring a first device to have (i) a first gate for receiving an input voltage ranging from up to twice a first supply voltage with respect to a second supply voltage to at least said second supply voltage, (ii) a first drain for receiving said first supply voltage, and (iii) a first source coupled to ~~an~~ a first output; and

configuring a first resistive element to have (i) a first side coupled to said first source and (ii) a second side for receiving said second supply voltage, wherein said first device and said first resistive element are arranged such that a maximum voltage drop across a gate oxide of said first device does not exceed a difference between said first supply voltage and said second supply voltage and a voltage drop from said first gate to said first output is non-linear as a function of said input voltage.

12. (PREVIOUSLY CANCELLED)

13. (CURRENTLY AMENDED) The method according to claim 11, wherein said first device is configured in a source-follow configuration.

14. (CURRENTLY AMENDED) The method according to claim 11, wherein said first device comprises an NMOS device.

15. (CURRENTLY AMENDED) The method according to claim 11, wherein said first device comprises a PMOS device.

16. (CURRENTLY AMENDED) The method according to claim 11, wherein said first device comprises a native NMOS device.

17. (CURRENTLY AMENDED) The method according to claim 11, wherein said first device comprises a native PMOS device.

18. (PREVIOUSLY AMENDED) An apparatus comprising:

a first stage comprising (A) a first device comprising (i) a first gate configured to receive an input voltage ranging from greater than a first supply voltage to at least a second supply voltage, (ii) a first drain configured to receive said second supply voltage, and (iii) a first source coupled to a first output, and (B) a first resistive element having (i) a first side coupled to said first source and (ii) a second side configured to receive said first supply voltage; and

a second stage comprising (A) a second device comprising (i) a second gate coupled to said first output, (ii) a second drain configured to receive said first supply voltage, and (iii) a second

source coupled to a second output, and (B) a second resistive element having (i) a first side coupled to said second source and (ii) a second side configured to receive said second supply voltage, wherein said apparatus is arranged such that a maximum voltage drop across a gate oxide of said first device does not exceed a difference between said first supply voltage and said second supply voltage.

19. (CURRENTLY AMENDED) The apparatus according to claim 1, further comprising:

~~a second device comprising (i) a second gate configured to receive said input voltage, (ii) a second drain configured to receive said second supply voltage, and (iii) a second source coupled to a second output;~~

~~a second resistive element having (i) a first side coupled to said second source and (ii) a second side configured to receive said first supply voltage; and~~

a multiplexer configured to multiplex said first output and ~~said~~ a second output to a third output.

20. (CURRENTLY AMENDED) An apparatus comprising:

a first stage comprising (A) a first device comprising (i) a first gate configured to receive an input voltage ranging from greater than a first supply voltage to at least a second

supply voltage, (ii) a first drain configured to receive said first supply voltage, and (iii) a first source ~~coupled~~ directly connected to an output, and (B) a first resistive element having (i) a first side coupled to said first source and (ii) a second side configured to receive said second supply voltage; and

a second stage comprising (A) a second device comprising (i) a second gate configured to receive said input voltage, (ii) a second drain configured to receive said second supply voltage, and (iii) a second source ~~coupled~~ directly connected to said output, and (B) a second resistive element having a first side coupled to said second source and a second side configured to receive said first supply voltage, wherein said apparatus is arranged such that a maximum voltage drop across each gate oxide of said first device and said second device does not exceed a difference between said first supply voltage and said second supply voltage.

21. (NEW) The apparatus according to claim 19, further comprising a second device having (i) a second gate configured to receive said input voltage, (ii) a second drain configured to receive said second supply voltage, and (iii) a second source coupled to said second output

22. (NEW) The apparatus according to claim 21, further comprising a second resistive element having (i) a first side

coupled to said second source and (ii) a second side configured to receive said first supply voltage.

23. (NEW) The method according to claim 11, further comprising the step of:

multiplexing said first output and a second output to a third output.

24. (NEW) The method according to claim 23, further comprising the step of:

configuring a second device to have (i) a second gate for receiving said input voltage, (ii) a second drain for receiving said second supply voltage, and (iii) a second source coupled to said second output.

25. (NEW) The method according to claim 24, further comprising the step of:

configuring a second resistive element to have (i) a first side coupled to said second source and (ii) a second side for receiving said first supply voltage.

26. (NEW) The apparatus according to claim 18, wherein said second stage is configured to cancel a voltage level shift at

said first output relative to said input voltage caused by a threshold voltage of said first device.